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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,734	04/13/2001	Masami Shirosaki	50088-057	6428

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EXAMINER
MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/833,734	SHIROSAKI ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-10 and 12-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10 and 12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's cancellation to claims 1-5 and 11 is acknowledged. Claims 19-22 are newly added. Thus, claims 6-10 and 12-22 are pending in this application.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/21/2003 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh et al. (U.S. 5,994,181) in view of the applicants admitted prior art in the instant application and DeBoer et al. (U.S. 6,046,093).

In reference to claims 6, 7 and 19, Hsieh et al. (Figs.1-10c) in a related method to form DRAM capacitors teach the steps of forming a contact hole (46) which penetrates an interlayer insulating film (38, 40) formed on a semiconductor substrate (1); forming an electric conductive film (48) on said interlayer insulating film (38, 40) whereby said

contact hole (46) is filled to obtain a contact to said substrate (1); forming an insulating film (51) on said electric conductive film (48); patterning by an anisotropic etching said insulating film (51) and said electric conductive (48) film to form a core (51) and the bottom portion; forming a side-wall configuration (54a) on the side of said core and said bottom portion wherein said configuration (54) can be roughened by using hemispherical grained silicon (column 4, lines 50-52), and wherein said configuration is formed by forming a conductive film (54) on the side walls of said core (51) and said bottom portion, and conducting an etching of said conductive film (54) to form said side wall configuration; removing said core; forming a dielectric film (60) to cover said configuration storage node comprising the configuration portion and said bottom portion; and forming a cell plate (62c) on said dielectric film (60), whereby a capacitor constituted by said configuration storage node, said dielectric film (60) and said cell plate (62) is formed (column 3, line 10 – column 5, line 35).

Hsieh et al. fail to teach that the configuration of the lower electrode is cylindrical. However, the prior art (Figs.6 and 7) teaches forming a DRAM capacitor structure in which the lower electrode (5a) is cylindrical (page 2, lines 1-12). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hsieh et al. and the prior art to enable configuring the outer wall of the capacitor of Hsieh et al. according to the teachings of the prior art because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of configuring the outer wall of Hsieh et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Hsieh et al. in combination with prior art fail to expressly teach roughening the outer wall of the cylindrical storage electrode by performing the sequential steps of forming a film comprising amorphous silicon on said core and said bottom portion; roughening the outer wall of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching patterning to form a side-wall-like cylindrical portion at the side of said core and said bottom portion.

However, DeBoer et al. (Figs.12-16) in a related method to form DRAM capacitors teach the step of roughening the outer wall of a storage electrode (70a), wherein said step comprises the sequential steps of forming a film comprising amorphous silicon on said core and said bottom portion (column 5, lines 25 – 65); roughening an outer wall of said of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching patterning to form a side-wall-like cylindrical portion at the side of said core and said bottom portion (column 4, line 7 – column 5, line 65 and column 7, lines 19-30).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hsieh et al. and the prior art with DeBoer et al. to enable the roughened surface of the cylindrical capacitor of Hsieh et al. and the prior art to be performed according to the teachings of DeBoer et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed roughening step of Hsieh et al. and DeBoer et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claims 8-10, the combination of Hsieh et al., the prior art and DeBoer et al. teach wherein the roughening of the outer surface of the amorphous silicon is performed by a heat treatment with the use of silane and the inner wall having a roughened outer wall was originally constituted by amorphous silicon, wherein said heat treatment is preceded by treating the outer surface of said amorphous silicon with hydrofluoric acid (see DeBoer et al., column 4, line 7 – column 5, line 65).

5. Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh et al. ('181) in view of the applicants admitted prior art in the instant application and Dennison et al. (U.S. 5,061,650).

Hsieh et al. (Figs.1-10c) in a related method to form DRAM capacitors teach the steps of forming a contact hole (46) which penetrates an interlayer insulating film (38, 40) formed on a semiconductor substrate (1); forming an electric conductive film (48) on said interlayer insulating film (38, 40) whereby said contact hole (46) is filled to obtain a contact to said substrate (1); forming an insulating film (51) on said electric conductive film (48); patterning by an anisotropic etching said insulating film (51) and said electric conductive (48) film to form a core (51) and the bottom portion; forming a side-wall configuration (54a) on the side of said core and said bottom portion wherein said configuration (54) can be roughened by using hemispherical grained silicon (column 4, lines 50-52), and wherein said configuration is formed by forming a conductive film (54) on the side walls of said core (51) and said bottom portion, and conducting an etching of said conductive film (54) to form said side wall configuration; removing said core; forming a dielectric film (60) to cover said configuration storage node comprising the

configuration portion and said bottom portion; and forming a cell plate (62c) on said dielectric film (60), whereby a capacitor constituted by said configuration storage node, said dielectric film (60) and said cell plate (62) is formed (column 3, line 10 – column 5, line 35).

Hsieh et al. fail to teach that the configuration of the lower electrode is cylindrical. However, the prior art (Figs.6 and 7) teaches forming a DRAM capacitor structure in which the lower electrode (5a) is cylindrical (page 2, lines 1-12). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hsieh et al. and the prior art to enable configuring the outer wall of the capacitor of Hsieh et al. according to the teachings of the prior art because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of configuring the outer wall of Hsieh et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Hsieh et al. and the prior art fail to teach forming a dielectric film on said cylindrical storage node comprising said cylindrical portion and said bottom portion within which said core remains. However, Dennison et al. (Fig.19) in a related method to form a stacked capacitor teach forming a dielectric film (48) on a storage node comprising a sidewall portion (42) and a bottom portion (34) within which a core (38) remains (column 6, lines 18 – 23). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hsieh et al. and Dennison et al. to enable the dielectric film formation step of Hsieh et al. the prior art to be performed according to the teachings of Dennison et al. because one of ordinary skill in the art at

the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed dielectric film formation step of Hsieh et al. and the prior art and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

6. Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh et al. ('181) in view of the prior art and Dennison et al. ('650) as applied to claim 12 above, and further in view of DeBoer et al. (U.S. 6,046,093).

Hsieh et al. in combination with prior art fail to expressly teach roughening the outer wall of the cylindrical storage electrode by forming a film comprising amorphous silicon on said core and said bottom portion; roughening an wall surface of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching patterning to form a side-wall-like cylindrical portion at the side of said core and said bottom portion, wherein the roughening of the outer wall of the amorphous silicon is performed by a heat treatment with the use of silane and the inner wall having a roughened outer wall was originally constituted by amorphous silicon, wherein said heat treatment is preceded by treating the outer surface of said amorphous silicon with hydrofluoric acid.

However, DeBoer et al. (Figs.12-16) in a related method to form DRAM capacitors teach the step of roughening the outer wall of a storage electrode (70a), wherein said step comprises forming a film comprising amorphous silicon on said core and said bottom portion; roughening an outer surface of said of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching

patterning to form a side-wall-like cylindrical portion at the side of said core and said bottom portion, wherein the roughening of the outer surface of the amorphous silicon is performed by a heat treatment with the use of silane and the inner wall having a roughened outer wall was originally constituted by amorphous silicon, wherein said heat treatment is preceded by treating the outer surface of said amorphous silicon with hydrofluoric acid (column 4, line 7 – column 5, line 65 and column 7, lines 19-30). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hsieh et al. and the prior art with DeBoer et al. to enable the roughened surface of the cylindrical capacitor of Hsieh et al. and the prior art to be performed according to the teachings of DeBoer et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed roughening step of Hsieh et al. and DeBoer et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

7. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh et al. ('181) in view of Khamankar et al. (U.S. 6,197,653 B1) and DeBoer et al. ('093).

Hsieh et al. (Figs.1-10c) in a related method to form DRAM capacitors teach the steps of forming a contact hole (46) which penetrates an interlayer insulating film (38, 40) formed on a semiconductor substrate (1); forming an electric conductive film (48) on said interlayer insulating film (38, 40) whereby said contact hole (46) is filled to obtain a contact to said substrate (1); forming an insulating film (51) on said electric conductive

film (48); patterning by an anisotropic etching said insulating film (51) and said electric conductive (48) film to form a core (51) and the bottom portion; forming a side-wall configuration (54a) on the side of said core and said bottom portion wherein said configuration (54) can be roughened by using hemispherical grained silicon (column 4, lines 50-52), and wherein said configuration is formed by forming a conductive film (54) on the whole side walls of said core (51) and said bottom portion, and conducting an etching of said conductive film (54) to form said side wall configuration; removing said core; forming a dielectric film (60) to cover said configuration storage node comprising the configuration portion and said bottom portion; and forming a cell plate (62c) on said dielectric film (60), whereby a capacitor constituted by said configuration storage node, said dielectric film (60) and said cell plate (62) is formed (column 3, line 10 – column 5, line 35).

Hsieh et al. fail to teach forming a cylindrical portion on the side of said core and said bottom portion wherein an outer wall of said cylindrical portion is roughened, comprising forming an amorphous silicon film on said core and said bottom portion; conducting an anisotropic etching of said amorphous silicon film to form said cylindrical portion having a side-wall like shape at the side of said core and said bottom portion so as to cover whole circumferential areas of said core and said bottom portion by said cylindrical portion; and roughening whole said outer wall of said cylindrical portion covering the whole circumferential areas of said core and said bottom portion by forming silicon grains.

However, Khamankar et al. (Figs.1a-1f) in a related method to form DRAM devices teach forming a cylindrical capacitor portion (see Figs.1a-1b) on a side of a core (Fig.2e-2f) and a bottom portion (105) wherein an outer wall of said cylindrical portion is roughened, comprising forming a silicon film (104) on said core and said bottom portion (105); and roughening whole said outer wall of said cylindrical portion (see Fig.1a) covering the whole circumferential areas of said core and said bottom portion by forming silicon grains (102) (column 2, line 47 – 3, line 46).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hsieh et al. and Khamankar et al. to enable the side wall roughening step of Hsieh et al. to be performed according to the teachings of Khamankar et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed roughening step of Hsieh et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Hsieh et al. in combination with Khamankar et al. fail to expressly teach roughening the outer wall of the cylindrical storage electrode by performing the sequential steps of forming a film comprising amorphous silicon on said core and said bottom portion; roughening the outer wall of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching patterning to form a side-wall-like cylindrical portion at the side of said core and said bottom portion.

However, DeBoer et al. (Figs.12-16) in a related method to form DRAM capacitors teach the step of roughening the outer wall of a storage electrode (70a),

wherein said step comprises the sequential steps of forming a film comprising amorphous silicon on said core and said bottom portion (column 5, lines 25 – 65); roughening an outer wall of said of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching patterning to form a side-wall-like cylindrical portion at the side of said core and said bottom portion (column 4, line 7 – column 5, line 65 and column 7, lines 19-30). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Hsieh et al. and the prior art with DeBoer et al. to enable the roughened surface of the cylindrical capacitor of Hsieh et al. and the prior art to be performed according to the teachings of DeBoer et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed roughening step of Hsieh et al. and DeBoer et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Response to Arguments

8. Applicant's arguments filed 10/21/2003 have been fully considered but they are not persuasive.

In reference to claim 7, applicants argue, "...Applicants submit that Hsieh et al., AAPA and DeBoer et al., either individually or in combination, do not teach or suggest the limitation "the inner wall of the cylindrical portion having the roughened outer wall is constituted by amorphous silicon." This is so because DeBoer discloses a feature that the amorphous silicon layer is crystallized (column 4, lines 19-20), a feature contrary to that recited in claim 7... Thus, the teachings of Hsieh et al., AAPA and DeBoer et a1.,

either individually or in combination, would not have suggested each and every limitation of claim 7..."In response to this argument, applicants assert that DeBoer et al. teach crystallizing the amorphous silicon layer. However, at the moment of the roughening of the outer wall of the capacitor, the inner wall is constituted by amorphous silicon (DeBoer et al., column 5, lines 26 – 65). Furthermore, the claim is open to other limitations such as rendering the amorphous silicon into polysilicon during a downstream process as taught by DeBoer (column 4, lines 19-20) because of the comprising language. Therefore, the rejection is deemed to be proper.

Also, applicants argue, "...the Examiner did not show any realistic motivation to impel a person skilled in the art to modify the device obtained by combining Hsieh et al., AAPA and DeBoer et al., based on the teaching of Dennison et al...Dennison et al. discloses that "FIG 19 illustrates an alternate embodiment whereby second dielectric laver 38 is not removed prior to application of the capacitor dielectric layer 48 and upper poly plate layer 50. (emphasis added) (column 6, lines 18-21)...Dennison et al. also discloses that "Removal of laver 38 is preferred to further maximize the exposed area for capacitance by utilizing the outer sides of rings 42" (emphasis added) (column 6, lines 21-23)...It can therefore be considered that Dennison et al. recommends to remove the "core."...since Hsieh et al. and DeBoer et al. teach that the "core" is removed and Dennison et al. teaches that removal of the "core" (layer 38) is preferred, there is no requisite realistic motivation to modify Hsieh et al., AAPA and DeBoer et al. to have the "core" and the Examiner did not show any factual basis supporting such motivation..." This argument is respectfully traversed because, although not taught as a

preferred embodiment, Dennison et al. teach this embodiment nonetheless, and disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments. In re Susi, 169 USPQ 423 (CCPA 1971). "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." In re Gurley, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994). A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments. Merck & Co. v. Biocraft Laboratories, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989). Even a teaching away from a claimed invention does not render the invention patentable. See Celeritas Technologies Ltd. v. Rockwell International Corp., 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir. 1998), where the court held that the prior art anticipated the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed." To further clarify, a prior art opinion that a claimed invention is not preferred for a particular limited purpose, does not preclude utility of the invention for that or another purpose, or even preferability of the invention for another purpose.

Conclusion

9. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November

1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
1/6/04

George Fourson
Primary Examiner